D. Johnson
#6 3-28-02
Priority Papers

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No: 27656/37751

PATENT APPLICATION TRANSMITTAL UNDER 37 C.F.R. 1.53

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): PIAZZI, Francesco

Title: RF Receiver with Power Off Control

1. Type of Application

☒ This is a new application for a
- ☒ utility patent.
- ☐ design patent.

☐ This is a continuation-in-part application of prior application no.

2. Application Papers Enclosed

1 Title Page
8 Pages of Specification (excluding Claims, Abstract, Drawings & Sequence Listing)
3 Page(s) of Claims
1 Page(s) of Abstract
2 Sheet(s) of Drawings (Figs. 1 to 3)
- ☒ Formal
- ☐ Informal

Page(s) of Sequence Listing

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this Patent Application Transmittal and the documents referred to as enclosed therewith are being deposited with the United States Postal Service on **October 9, 2001**, in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231 utilizing the "Express Mail Post Office to Addressee" service of the United States Postal Service under Mailing Label No. EK657819567US.

Richard Zimmermann

3. **Declaration or Oath**

☒ Enclosed

☐ Executed by (check all applicable boxes)

☐ Inventor(s)

☐ Legal representative of inventor(s) (37 CFR 1.42 or 1.43)

☐ Joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached

☐ The petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 are enclosed. See Item 5D below for fee.

☒ Not enclosed - the undersigned attorney or agent is authorized to file this application on behalf of the applicant(s). An executed declaration will follow.

4. **Small Entity Status**

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A small entity statement is(are) attached.

5. **Additional Papers Enclosed**

☐ Preliminary Amendment

☐ Information Disclosure Statement

☐ Declaration of Biological Deposit

☐ Computer readable copy of sequence listing containing nucleotide and/or amino acid sequence

☐ Microfiche computer program

☐ Associate Power of Attorney

☐ Verified translation of a non-English patent application

☐ An assignment of the invention

☐ Request and Certification Under 35 U.S.C. 122(b)(2)(B)(i)

☒ Return receipt postcard

☐ Other

6. **Priority Applications Under 35 USC 119**

Certified copies of applications from which priority under 35 USC 119 is claimed are listed below and

☒ are attached.

☐ will follow.

COUNTRY	APPLICATION NO.	FILED
EPO	00810933.2	10 October 2000

7. **Filing Fee Calculation (37 CFR 1.16)**

A. ☒ **Utility Application**

CLAIMS AS FILED - INCLUDING PRELIMINARY AMENDMENT (IF ANY)						
			SMALL ENTITY		OTHER THAN A SMALL ENTITY	
	NO. FILED	NO. EXTRA	RATE	FEE	RATE	FEE
BASIC FEE				$355.00		$740.00
TOTAL	14 -20	=	X 9 =	$	X 18 =	$
INDEP.	3 - 3	=	X 40 =	$	X 80 =	$
☐ First Presentation of Multiple Dependent Claim			+ 135 =	$	+ 270 =	$
			Filing Fee:	$	OR	$740.00

B. ☐ **Design Application ($160.00/$320.00)** Filing Fee: $ _____

C. ☐ **Plant Application ($245.00/$490.00)** Filing Fee: $ _____

D. **Other Fees**

☐ Recording Assignment [Fee -- **$40.00** per assignment] $ _____

☐ Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached [Fee -- **$130.00**] $ _____

☐ Other $ _____

Total Fees Enclos d **$740.00**

8. **Meth d of Payment of Fees**

☒ Enclosed check in the amount of: $740.00

☐ Charge Deposit Account No. 13-2855 in the amount of: $_____
A copy of this Transmittal is enclosed.

☐ Not enclosed

9. **Deposit Account and Refund Authorization**

The Commissioner is hereby authorized to charge any deficiency in the amount enclosed or any additional fees which may be required during the pendency of this application under 37 CFR 1.16 or 37 CFR 1.17 or under other applicable rules (except payment of issue fees), to Deposit Account No. 13-2855. A copy of this Transmittal is enclosed.

Please refund any overpayment to Marshall, Gerstein & Borun at the address below.

10. **Correspondence Address**

Customer No.: 04743

Respectfully submitted,

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By: 
Jeffery S. Sharp
Reg. No: 31,879

October 9, 2001

Europäisches Patentamt	European Patent Office	Office européen des brevets

Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00810933.2

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

I.L.C. HATTEN-HECKMAN

DEN HAAG, DEN
THE HAGUE, 30/08/01
LA HAYE, LE

Eur päisches Patentamt | European Patent Office | Office européen des brevets

Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.:
Demande n°: 00810933.2

Anmeldetag:
Date of filing:
Date de dépôt: 10/10/00

Anmelder:
Applicant(s):
Demandeur(s):
TCHip Semiconductor SA
6928 Manno
SWITZERLAND

Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
Electronic circuit and RF receiver with power save control

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

Internationale Patentklassifikation:
International Patent classification:
Classification internationale des brevets:
H04B1/16, H02J9/00

Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/TR
Etats contractants désignés lors du depôt:

Bemerkungen:
Remarks:
Remarques:

Electronic circuit and RF receiver with power save control

The invention relates to an electronic circuit and a radio frequency receiver according to the preamble of the independent claims.

It has been known to provide electronic circuits with power save units for switching the circuits off when they are not used. When switching the circuits off, it may be required or desirable that their settings are saved. E.g. when switching a TV off by a remote control, its current loudness settings should be preserved. For this purpose, a control voltage controlling the loudness is stored in a digital memory, from where it is fed to an D/A-converter when the device is switched back on. This, however, requires additional circuitry.

Furthermore, it has been know to preserve energy in radio frequency receivers by switching the receiver section on and off, in particular in receivers of digital data with a know time structure. In such receivers, the settings of the receiver section, e.g. the control voltage of a VCO in a PLL, are usually lost during power-off periods. When these components are switched back on, some time passes before the settings have been re-established.

Hence, the problem to be solved by the present invention is to provide an electronic circuit and an RF receiver of the type mentioned above that maintain their settings while being switched off without requiring additional complicated circuitry.

This problem is solved by the independent claims.

To store the setting, the corresponding control voltage is stored in a storage capacitor. This obviates the need for providing a digital memory and a D/A-converter. Since the control voltage needs not be con-

verted to digital information and back, circuitry remains simple and power consumption is reduced.

For a reliable storage of the control voltage, a discharge time of the capacitor during switch-off should be much larger than a typical switch-off time.

To increase storage time, an electronic switch can be provided for disconnecting the capacitor from at least part of the circuit elements while they are switched off. Alternatively or in addition to that, an active hold circuit can be used for maintaining the voltage over the capacitor.

The technology described here is particularly useful for RF receivers. When part of an RF receiver is switched off for reducing power consumption, its settings can be maintained using capacitive storage.

In particular, RF receivers usually comprise down-converters, where the incoming signal is mixed to a reference frequency. The reference frequency is usually generated by a VCO in a PLL. If such a circuit is switched off and back on, it requires some time to regain stable reference frequency unless the voltage controlling the VCO is stored.

Further preferred embodiments as well as applications of the invention are described in the dependent claims as well as in the following description making reference to the enclosed figures, wherein

Fig. 1 shows a circuit diagram of an RF receiver,

Fig. 2 part of the automatic gain control circuit, and

Fig. 3 part of the PLL circuit.

A preferred embodiment of the invention is an RF-receiver shown in Fig. 1. The receiver shown here is used for receiving the signal of GPS satellites at 1575.42 MHz, but the same technique can be applied to other type of radio receivers, in particular for digital signals.

The receiver comprises an antenna 1 with low noise amplifier 2 and an input filter 3. The signal from input filter 3 is fed to a frequency mixer 4, which mixes the carrier at 1575.42 MHz with a frequency of 1554.96 MHz to generate a downconverted first IF signal at 20.46 MHz. The first IF signal is filtered in a first IF filter 5 and fed to a second mixer 6, where it is mixed with a frequency of 16.368 MHz to generate a second downconverted IF signal at 4.092 MHz. The second IF signal is fed through a second IF filter 7 and to a adjustable amplifier 8. The output of adjustable amplifier 9 is fed to an A/D-converter 9 which generates a digital value of two bits SGN and MAG giving the sign and magnitude of the signal. The magnitude bit is analyzed by an adjustable gain control (AGC) 10 to set the gain of adjustable amplifier 8.

The design of AGC 10 is shown in Fig. 2. It comprises a switch control unit 20 controlling a switch 21. In a first state, switch 21 connects a capacitor C1 via a current source 22 to the positive supply voltage Vdd. In a second state, switch 21 connects capacitor C1 via a current source 23 to the negative supply voltage or ground. In a thirds state, switch 23 is in high impedance state. The voltage U1 over C1 is fed as a control voltage to the high impedance input of a buffer 24, the output of which controls amplifier 8, wherein a lower voltage U1 corresponds to a higher amplification in amplifier 8.

In normal operation, if MAG is 1, switch 21 is in its first state and, if MAG is 0, switch 21 is in its second state, i.e. the voltage over capacitor C1 is proportional to the average value of MAG. If the average value of MAG is large, voltage U1 increases, thereby decreasing the amplification of adjustable amplifier 8 and vice versa. The gain loop is adjusted such that it tries to hold MAG at an average value of 0.33.

The circuit of Fig. 1 further comprises a Quartz oscillator 11 operating at 16.368 MHz. It gener-

ates the reference frequency for second mixer 6. Furthermore, it provides a frequency base for a PLL. The PLL comprises a phase and frequency comparator 12 for comparing the Quartz oscillator frequency divided by 16 to the PLL's frequency divided by 1520. The output of comparator 12 is fed to a low pass filter comprising storage capacitors C2, C3, the voltage U2 over which is the control voltage for the resonance frequency of a tank circuit 13 of a VCO 14. By this arrangement, the VCO's frequency is kept at 1554.96 MHz, the reference frequency for first mixer 4.

The design of the part of the PLL that drives capacitors C2, C3 is shown in Fig. 3. It comprises a switch control unit 26 controlling a switch 27. In a first state, switch 27 connects capacitors C2, C3 via a current source 29 to the positive supply voltage Vdd. In a second state, switch 27 connects capacitors C2, C3 via a current source 30 to the negative supply voltage or ground. In a third state, switch 27 is in high impedance state. If the comparator finds that the VCO's frequency is too low, switch 27 is primarily set to its first state, thereby increasing voltage U2 over the capacitors, while, if the VCO's frequency is too high and for decreasing voltage U2, switch 27 is primarily in its second state.

The circuit of Fig. 1 comprises a power save unit 15. The purpose of this power save unit is to temporarily switch off the circuits of the RF receiver for conservation of power. The position and length of the switch-off periods can e.g. be selected according to a known temporal structure of the incoming signal or according to requirements of the user of the RF receiver.

Power save unit 15 switches off power supply to mixers 4, 6, amplifiers 2, 8, ADC 9 and AGC 10, as well as to the PLL (comparator 12, VCO 14 and frequency dividers) by issuing a control signal PWR SAVE. Typical

power-off periods may e.g. have a duration between 1 ms and several seconds.

After a power-off period, power to the circuits of the RF receiver is switched back on and the RF receiver should become operational quickly. Without special provisions, the start-up time of the receiver would be limited by the time it takes for the circuit to re-establish its dynamic settings. These settings are the amplification of adjustable amplifier 8 as well as the frequency of the PLL. To reduce the start-up time, the circuit of Fig. 1 is designed to store these settings as control voltages U1, U2 over the capacitors C1 and C2 or C3. While power is off, the load impedance offered by the circuits to these capacitors is high enough to make the discharge time of the capacitors much longer than a typical power-off period. A typical power-off period is e.g. limited by a few seconds, while the discharge time is e.g. 100 times as large.

It must be noted that the capacitors C1, C2 and C3 serve two purposes. First they act as low pass filters or integraters in their corresponding feed-back loops (ACG and PLL), second they store the setting of the loop during power-off.

To achieve high discharge times, switches 21 and 27 are both set to their third, high impedance state while the signal PWR SAVE indicates that the circuit is switched off.

To reach even higher discharge times, the capacities of the capacitors can be increased where possible. In addition or alternatively to this, active hold circuits can be used to maintain the voltage of the capacitors during power-off periods. In such a circuit, the storage capacitor can e.g. be arranged in the negative feedback loop between the amplifier output and its inverting input.

By storing the control voltages in the capacitors, the circuit can be switched back on quickly because its settings are maintained.

The principle described here can be used in other electronic circuits having settings that can be controlled by control voltages. In such circuits, the control voltages can be stored in suitable capacitors while power is shut down. The technique shown here is especially suited for PLL circuits in any application or for storing the amplification setting or setpoint of an adjustable RF or LF amplifier. It can also be used for storing the settings of any feedback loops.

In the embodiment described above, power save unit 15 is controlled automatically, i.e. the time and duration of the switch-off periods are not directly determined by the user. However, power save unit 15 could also be controlled by the user directly.

Claims

1. An electronic circuit comprising

circuit elements a setting of which is controlled by at least one control voltage (U1, U2),

a power save unit (15) for switching off the circuit elements during power-off periods, and

a storage for storing the control voltage (U1, U2) while the circuit elements are switched off,

characterized in that the storage comprises a storage capacitor (C1; C2, C3) storing the controlvoltage.

2. The electronic circuit of one of the preceding claims wherein the storage comprises an electronic switch (21, 27) for disconnecting the capacitor (C1; C2, C3) from at least part of the circuit elements while the circuit elements are switched off.

3. The electronic circuit of one of the preceding claims wherein the storage comprises a hold circuit for actively maintaining the voltage over the capacitor (C1; C2, C3) while the circuit elements are switched off.

4. The electronic circuit of one of the preceding claims comprising at least one amplifier (8), wherein an amplification factor of the amplifier (8) is controlled by the control voltage (U1).

5. The electronic circuit of one of the preceding claims comprising at least one phase locked loop with a voltage controlled oscillator (13, 14), wherein the control voltage (U2) controls the frequency of the voltage controlled oscillator.

6. The electronic circuit of one of the preceding claims wherein the power save unit (15) is adapted to switch off the circuit elements for a typical time period, wherein, during switch-off, a discharge time of the capacitor (C1; C2, C3) is much larger than the typical time period.

7. The electronic circuit of one of the preceding claims wherein the capacitor (C1; C2, C3) is part of a low pass filter in a feed-back loop.

8. A radio frequency receiver comprising the electronic circuit of one of the preceding claims.

9. The radio frequency receiver of claim 8 comprising a frequency downconverter (4) for downconverting an incoming signal to an intermediate frequency and an oscillator circuit (14) being connected to the downconverter (4), wherein a frequency of the oscillator circuit (14) is being controlled by the control voltage and wherein the oscillator (14) is being switched on and off by the power save unit (15).

10. The radio frequency receiver of claim 9 wherein the oscillator circuit comprises a voltage controlled oscillator (13, 14) in a phase locked loop, wherein the frequency of the voltage controlled oscillator (13, 14) is being controlled by the control voltage.

11. The radio frequency receiver of one of the claims 8 - 10 wherein the power save unit (15) switches the electronic circuit on and off according to a temporal structure of a received radio signal.

Abstract

An RF receiver or another type of electronic circuit contains circuit elements a setting of which is controlled by at least one control voltage (U1, U2). Furthermore, a power save unit (15) is provided for switching off the circuit elements during power-off periods. While the circuit elements are switched off, the control voltage (U1, U2) is stored in storage capacitors (C1, C2, C3), which allows to start the circuit up quickly after a switch-off period.

(Fig. 1)

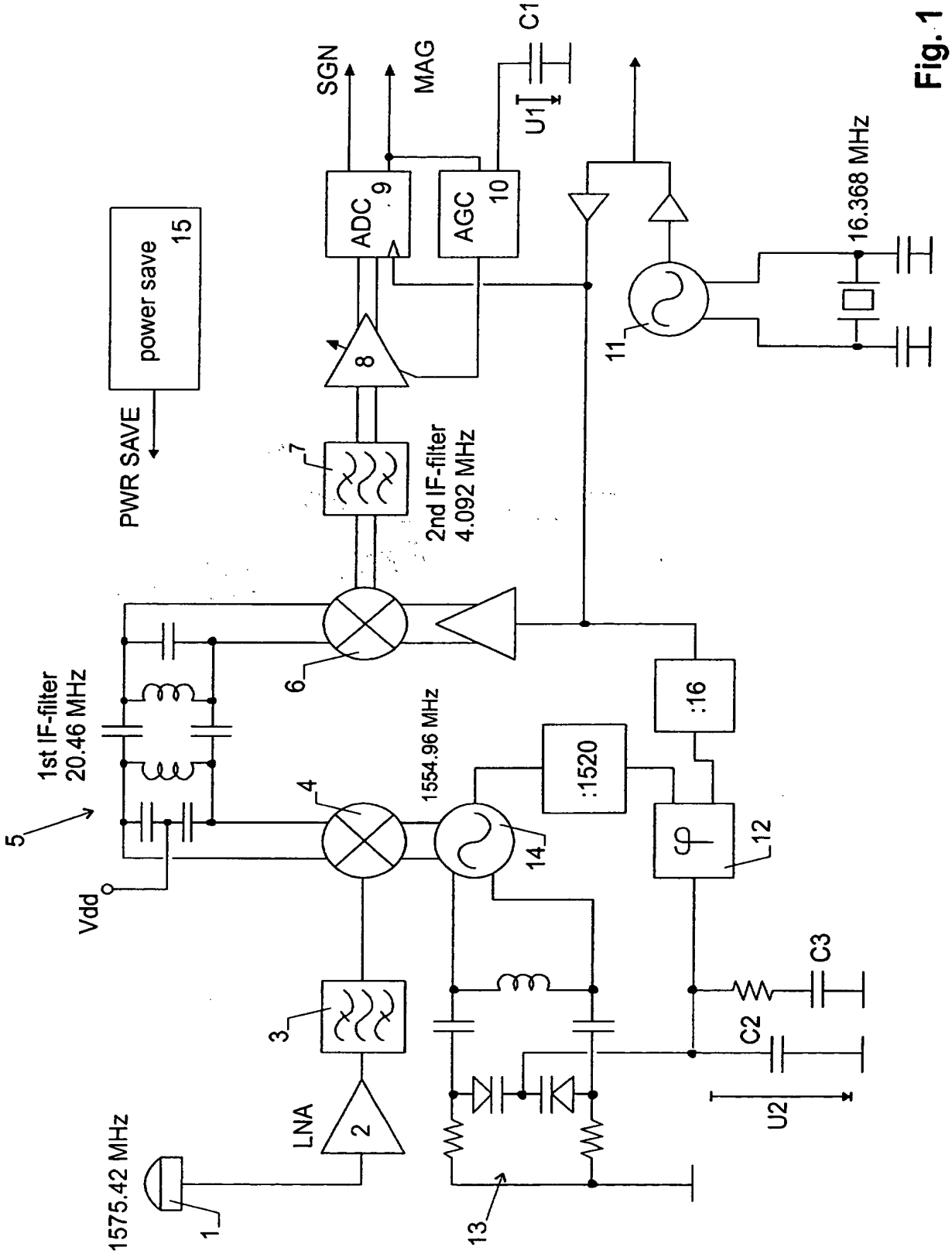
SGN
MAG
C1
U1
ADC 9
AGC 10
power save 15
PWR SAVE
8
7
2nd IF-filter 4.092 MHz
16.368 MHz
11
6
1st IF-filter 20.46 MHz
5
4
1554.96 MHz
:16
:1520
12
14
Vdd
3
C3
C2
U2
LNA
2
1575.42 MHz
1
13

Fig. 1

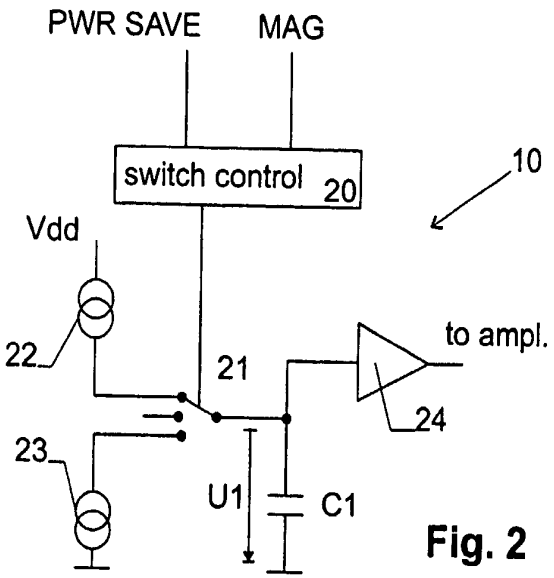

Fig. 2

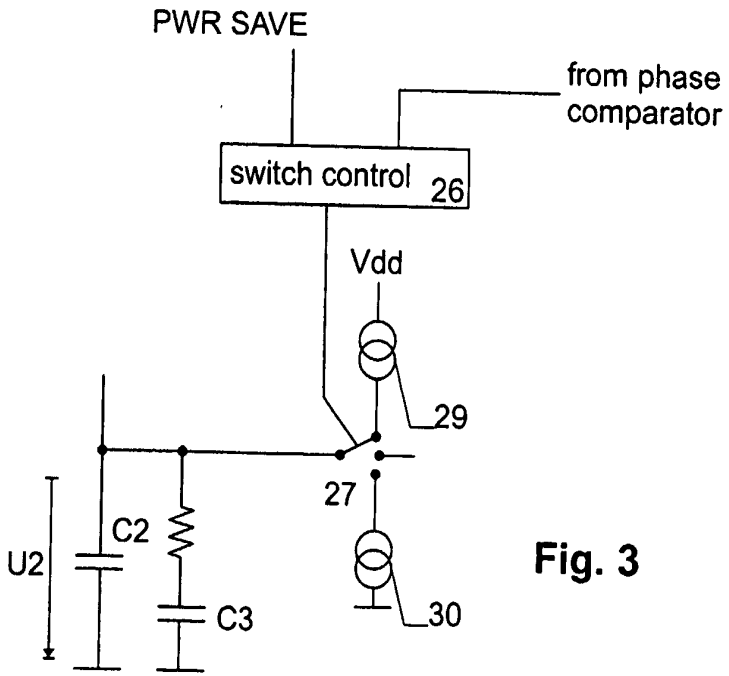

Fig. 3